Freescale Semiconductor, Inc.

CHAPTER 3 FUNCT

3.1 INTRODUCTION.....
3.2 EVB DESCRIPTION.....
3.3 MCU SUMMARY.....
3.3.1 32-Bit Central Processor Unit.....
3.3.2 Time Processor Unit.....
3.3.3 Queued Serial Module.....
3.3.4 Random Access Memory.....
3.3.5 External Bus Interface.....
3.3.6 Chip Selects.....
3.3.7 System Clock.....
3.3.8 Test Module.....
3.4 USER MEMORY.....
3.5 I/O CONNECTORS.....
3.5.1 64-Pin Expansion Connectors.....
3.5.2 Serial Communication Connectors....
3.5.3 Background Mode Interface Connecto
3.6 PFB DESCRIPTION.....
3.6.1 Floating-Point Coprocessor Socket (U
3.6.2 Logic Analyzer Connectors.....

CHAPTER 4 SUPP

4.1 INTRODUCTION.....
4.2 CONNECTOR SIGNAL DESCRIPTION

FIGU

2-1. EVB Connector, Switch, and Jumper Heac
2-2. Power Supply Connector (P7).....
2-3. Expansion Connector P6 Pin Assignments
2-4. Expansion Connector P7 Pin Assignments
3-1. EVB Block Diagram.....
3-2. EVB Memory Map.....

MPC5

EVALUATI

USER'S M

© MOTOROLA Inc., 19

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

Freescale Semiconductor, Inc.

MOTOROLA

Motorola reserves the right to make changes w
improve reliability, function, or design. Motorol
application or use of any product or circuit desc
under its patent rights nor the rights of others. M
authorized for use as components in systems inte
application in which the failure of the Motorola
injury or death may occur. Should Buyer pur
unintended or unauthorized application, Buye
officers, employees, subsidiaries, affiliates, and
damages, and expenses, and reasonable attorne
claim of personal injury or death associated wit
such claim alleges that Motorola was negligent r

Motorola and the Motorola logo are registered tr

Motorola Inc. is an Equal Opportunity/Affirmati

PowerPC is a trademark of International Busines

Freescale Semiconductor, Inc.

CONT

CHAPTER 1 GEN

1.1 INTRODUCTION.....
1.2 FEATURES.....
1.3 GENERAL DESCRIPTION .....
1.4 SPECIFICATIONS .....
1.5 EQUIPMENT REQUIRED.....

CHAPTER 2 HARDWARE PRE

2.1 INTRODUCTION.....
2.2 HARDWARE PREPARATION .....
2.2.1 Crystal Clock Select Header (J1) .....
2.2.2 Clock Source Select Header (J2).....
2.2.3 Keep Alive Power 2 Select Header (
2.2.4 Keep Alive Power 2 Select Header (
2.2.5 Burst Memory Select Header (J5)....
2.2.6 System Clock Selection Headers (J6
2.2.7 EVB LED Descriptions .....
2.2.8 Optional Memory Configuration.....
2.2.9 EVB Reset Switches.....
2.2.10 EVB DIP Switches .....
2.2.10.1 Chip Select Dip Switch (DS1).
2.3.10.2 Reset Data Dip Switches (DS2
2.2.10.3 DTE/DCE Settings .....
2.3 INSTALLATION INSTRUCTIONS.....
2.3.1 Host Computer – EVB Interconnecti
2.3.2 Background Mode Connector (P5)...
2.3.3 Power Supply – EVB Interconnectio
2.3.4 RS-232C – EVB Interconnection .....
2.3.5 EVB Expansion Connectors.....
2.3.6 Logic Analyzer Connectors.....
2.3.7 SCSI.....

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

1.3 GENERAL DESCRIPTION

The EVB is a low-cost tool for evaluating and
MPC505 MCU device is an advanced single-cl
functions. For more information refer to the Pow
Summary (MPC505TS/D).

The EVB includes a monitor/debugging program
the MPC505. You can debug user code under co
it (as either a Motorola S-record, COFF, or ELF

The Motorola S-record format lets you encode
transportation between computer systems. The tr
and the S-records easily edited. Refer to Append

The EVB has one host computer port (P4),
background debug mode port (P5). The ho
downloading S-records and communicating w
configure P4 as DTE or DCE. P4 is fixed at 19
EVB are RS-232C I/O ports. These two I/O po
communication. These ports can be configured a
terminal equipment (DTE) protocol via a set of
DTE a computer terminal). These serial ports ar
system monitor, MPCbug, does not require thes
1200 to 19200. P5 (10-pin berg) lets you comm
debug mode.

The EVB requires a user-supplied +5 Vdc powe
to +3.3 Vdc by the EVB on-board voltage con
MPC505 MCU.

The EVB comes with a 4 MHz crystal and a so
configured to use the 4 MHz crystal as the input
MHz (refer to paragraph 2.2.8).

All MPC505 MCU signals are available, unbu
analyzer connectors. The logic analyzer conne
during the development stage.

There are four flash memory devices (U24, U2
kilobytes of program storage memory. These de
You may program on-board flash memory us
program via the debug port and run the program

TAB

1-1. EVB Specifications .....
1-2. External Equipment Requirements .....
2-1. Jumper Header Types.....
2-2. MPFB Jumper Header Descriptions.....
2-3. MF and RFD Bits Required to Set Clock S
2-4. System Clock Source Configuration.....
2-5. Optional Memory Configuration.....
2-6. Chip Select Dip Switch (DS1) .....
2-7. Data Bus Reset Configuration Word.....
2-8. DS6 Communication Type Switch Setting
2-9. SCSI Port Parts List.....
4-1. SCSI Connector (not populated) .....
4-2. RS-232C I/O Connector P2 Pin Assignme
4-3. RS-232C I/O Connector P3 Pin Assignme
4-4. Host Computer Connector P4 Pin Assignn
4-5. Debug Mode Connector P5 Pin Assignme
4-6. P6 Expansion Connector Pin Assignments
4-7. Input Power Connector P7 Pin Assignmen
4-8. P8 Expansion Connector Pin Assignments
4-9. Logic Analyzer Connector POD1 Pin Assi
4-10. Logic Analyzer Connector POD2 Pin Assi
4-11. Logic Analyzer Connector POD3 Pin Assi
4-12. Logic Analyzer Connector POD4 Pin Assi
4-13. Logic Analyzer Connector POD5 Pin Assi
4-14. Logic Analyzer Connector POD6 Pin Assi
4-15. Logic Analyzer Connector POD7 Pin Assi

Freescale Semiconductor, Inc.

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

CHAP

GENERAL IN

1.1 INTRODUCTION

This manual provides general information, hard
support information for the MPC505EVB Evalu
PowerPC MPC505 RISC Microcontrollers.

1.2 FEATURES

EVB features include:

- MPC505 MCU running at 4-33 MHz
- 512 kilobytes of flash memory (may l
- 128 kilobytes of synchronous static R
- Serial port with 25-pin RS-232 conne
- MC68681 DUART providing two ser
- MC68HC711 MCU for the backgrou
- SCSI-2 port (optional)
- Expansion connectors for the MPC50
- 20-pin logic analyzer connectors for t
- 5-volt-to-3.3-volt converter for the M
- Reset data configuration switches
- Crystal or crystal oscillator operation

Freescale Semiconductor, Inc.

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

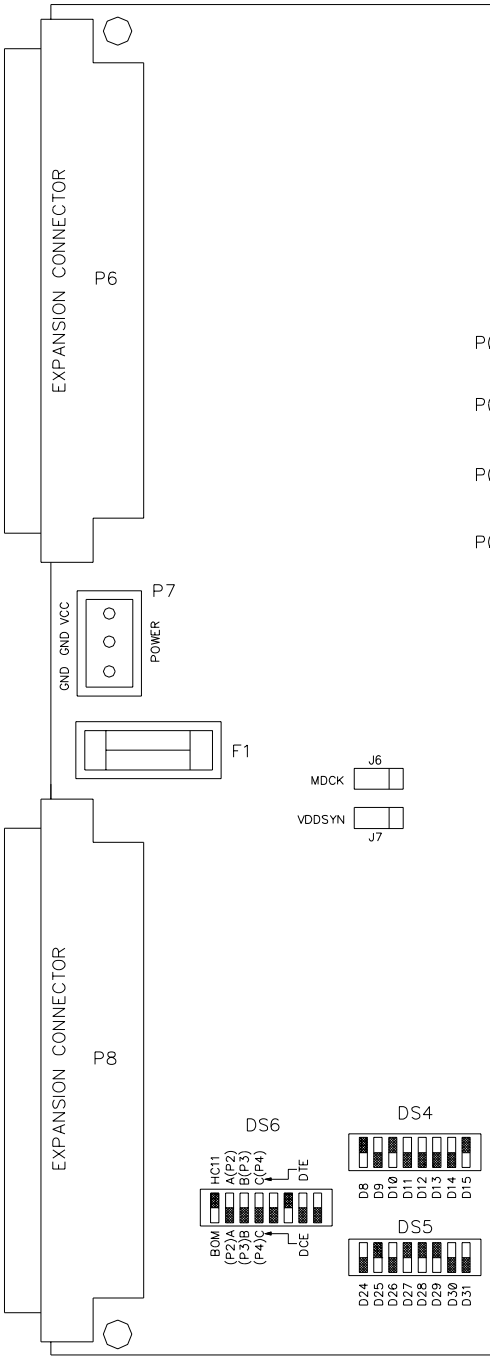


Figure 2-1. EVB Connector, Switch, a

to 2 megabytes by replacing the devices at lo
devices. The flash memory devices require +5 vo

There are a total of eight 52-pin PLCC sockets
U31, and U32) for synchronous static RAM (SSI
and lower words and organized for long-word (3
to as BANKx.

The SSRAM factory default for the EVB is 128
These devices have 9 nanosecond access times ar
be expanded to 256 kilobytes by replacing the
devices.

Alternately, you may increase the amount of on
U30, U31, and U32 with additional SSRAM dev
megabytes. (For information on increasing on-bo

The EVB includes an optional SCSI-2 port con
not provided, and the user may add them if the
are provided in Chapter 2.

1.4 SPECIFICATIONS

Table 1-1 lists the EVB specifications.

Table 1-1. EVB

Characteristics	
MCU	MP MP
I/O ports: I/O devices Host computer	 RS- RS-
Temperature: Operating Storage	+25 0 to 0 to
Relative humidity	0 to
Power requirements	+5 V
Dimensions:	9.1

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

Freescale Semiconductor, Inc.

1.5 EQUIPMENT REQUIRED

Table 1-2 lists the external equipment requireme

Table 1-2. External Eq

External E
+5 Vdc power supply
SUN host computer
RS-232C cable assembly

CHAP

HARDWARE PREPARATI

2.1 INTRODUCTION

This chapter provides unpacking instructions, ha
for the EVB. Chapter 6 is a description of the EV

2.2 HARDWARE PREPARATION

This paragraph describes the preparation of EV
ensure that the EVB components are properly co
shipped with factory-installed jumpers. Figure 2-
header locations. The EVB consists of:

- Dip switch DS1 lets you disconnect t
the target board.
- Dip switches DS2 through DS5 defin
- Dip switch DS6 sets P2 ,P3 ,P4 and fo
- Jumper headers J1 through J7 are for
2-2 and paragraphs 2.2.1 through 2.2.
- Connector P1 is a SCSI interface con
- Connectors P2 and P3 let you conne
purposes.
- Connector P4 is the serial port fo
computer. You must supply your own
- Connector P5 is the debug mode port
debug mode.
- Expansion connectors P6 and P8 let
board.
- Connector P7 is the EVB +5 Vdc pow
- POD1 through POD7 are 20-pin lo
MPC505 MCU signals.
- Switch SW1 lets you reset the MPC5
- Switch SW2 lets you reset the EVB.

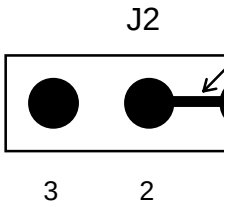
For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

Freescale Semiconductor, Inc.

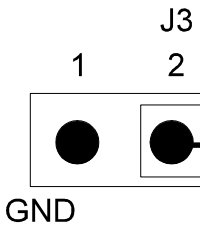
2.2.2 Clock Source Select Header (J2)

Use jumper header J2 to select either a crystal o
drawing below shows the factory configuratic
configuration selects the crystal clock source; cr
use the clock oscillator as the EVB clock, move
and 2 and remove the bus wire on J1 (see paragra
from the crystal clock circuit at location Y1 an
clock source. The frequency of the crystal clock
oscillator circuit can be as fast as 40 MHz.



2.2.3 Keep Alive Power 2 Select Header (J3

Jumper header J3 provides power to the MCU-i
pin. You may use either the on-board +3.3 Vc
external +3.3 Vdc power supply to J3 pins 2 ar
pins 2 and 3 will maintain MCU-internal RAM
an external power supply to VKAPWR2: remov
power supply ground to J3 pin 3 and +3.3 Vdc to



Fabri

CAU

Applying power to the EVB wi
power supply attached to J4 w
Always keep a jumper or an exter
pins 1 and 2. If using an external
before powering up the EVB.

Table 2-1. Jump

Jumper Header Type	Symbol	
two-pin with solder strap		Two-pin plate designated as soldered betw create a short
two-pin		Two-pin jumpe header numbe between the tw
two-pin with jumper		Two-pin jumpe jumper header
three-pin		Three-pin jum header numbe between two c
three-pin with jumper		Three-pin jum the jumper he configuration,

Table 2-2. MPFB Jump

Jumper Header	Type	
J1 Crystal clock sourcr select header (XTAL)	2 1 	Bus wire soldered betw on-board 4 MHz crystal Bus wire between pins 1 clock source as the MC
J2 Clock oscillator source select header (EXTAL)	3 2 1 	Bus wire between pins 1 source as the MCU EXT between pins 1 and 2 or Bus wire soldered betw on-board 4 MHz crystal
J3 Keep alive power 2 select header	3 2 1 	Jumper installed on pins active as long as power VKAPWR2 pin of the M +3.3 Vdc external powe internal RAM after EVB

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

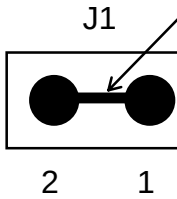
Freescale Semiconductor, Inc.

Table 2-2. MPFB Jumper He

Jumper Header	Type	
J4 Keep alive power 1 select header	3 2 1	Jumper installed on pins time base, and decreme EVB (+3.3 Vdc present +3.3 Vdc external powe maintains MCU-internal after EVB power is turne
J5		Unused
J6, System clock selection header	3 2 1	Jumper installed on pins J7 select the MCU clock the source of the systen
J7 System clock selection header	3 2 1	Jumper installed on pins J7 select the MCU clock

2.2.1 Crystal Clock Select Header (J1)

Jumper header J1 connects the crystal clock to t below shows the factory configuration: bus wir selects the crystal clock source; crystal in socket oscillator as the EVB clock, remove the bus wire and 3 to pins 1 and 2 (see paragraph 2.2.2). T crystal clock circuit at location Y1 and selects the The frequency of the crystal clock circuit is 4 MH can be as fast as 40 MHz.



The EVB comes with a 4 MHz crystal and a so configured to use the 4 MHz crystal as the input. MHz by setting the MF bits (bits 9-12) and RF 0x8007_FC50 (shown in Table 2-3).

Table 2-3. MF and RFD Bits

RFD [0:3]	CLKO			
	MF= X000 (X4)	MF= X001 (X5)	MF= X010 (X6)	MF= X0 (X
0 = 0000	16	20	24	2
1 = 0001	8	10	12	1
2 = 0010	4	5	6	
3 = 0011	2	2.5	3^2	3
4 = 0100	1	1.25	1.5	1.
5 = 0101	.5	.625	.75	.8
6 = 0110	.25	.313	.375	.4
7 = 0111	.125	.156	.188	.2

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

Freescale Semiconductor, Inc.

2.2.9 EVB Reset Switches

There are two reset switches on the EVB:

- Switch SW1 lets you reset the MPC5(
- Switch SW2 lets you reset the EVB.

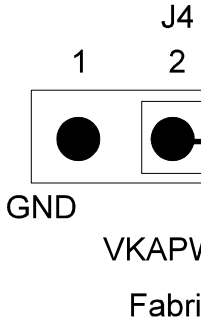
2.2.10 EVB DIP Switches

There are six DIP switches on the EVB (DS1 – D

- DS1 – Attaches the MCU chip selec devices. You may disable on-board c connectors (P6 and P8) to external me
- DS2, DS3, DS4, DS5 – Data Bus Res
- DS6 – On the EVB are 3 RS232 pc mode connector (P5). Each of the (defined by DS6 switches 2, 3 and 4) the RS-232 port or the debug mode cc

2.2.4 Keep Alive Power 2 Select Header (J4

Jumper header J3 provides power to the MCU modules via the MCU VKAPWR1 pin. You may pins 1 and 2) or connect an external +3.3 Vdc pc Vdc power supply on J4 pins 2 and 3 will mainta turned OFF. To attach an external power supply and 2, and connect the power supply ground to J4



CAU

Applying power to the EVB wi power supply attached to J4 w Always keep a jumper or an exter pins 1 and 2. If using an external before powering up the EVB.

2.2.5 Burst Memory Select Header (J5)

Unused.

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

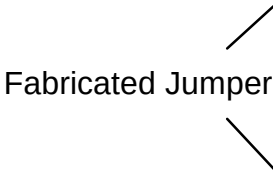
Freescale Semiconductor, Inc.

2.2.6 System Clock Selection Headers (J6 a

Jumper headers J6 and J7 let you define the s
(shown below) is for normal operation; a fabric
Table 2-4 for configuring the system clock sourc

Table 2-4. System Cloc

MODCLK (J6) Jumper Settings	VDDSYN Jumper Se
1 and 2 (default)	1 and 2 (d
2 and 3	1 and
1 and 2	2 and
2 and 3	2 and



2.2.7 EVB LED Descriptions

There are three LEDs on the EVB. Their functio

- LD1 – 3.3 Vdc power: ON = 3.3 Vdc
- LD2 – Debug Mode: ON = MPC505
- LD3 – +5 Vdc power: ON = power is

2.2.8 Optional Memory Configuration

There are eight 52-pin PLCC sockets on the EV
U32) for synchronous static RAM (SSRAM) c
lower words and organized for long-word (32 bi
BANKx. Table 2-5 shows on-board, memory co

Table 2-5. Optional M

Bank	Upper Word	Lower
BANK1	U29	U1
BANK2	U30	U2
BANK3	U31	U2
BANK4	U32	U2

The SSRAM factory default for the EVB is 128
(U19 and U29). You may increase the amou
increasing the memory in sockets U19 and U29
populating U20, U21, U22, U30, U31, and U32
The EVB can have up to 1 megabyte of on-board

Freescale Semiconductor, Inc.

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

Table 2-7. Data Bus Reset Co

Data Bus Bit	Configuration Function Effected	Effect o Mode Selec During Re
24	LEN	L-bus Memory m are enabled.
25	PRUMODE	Forces accesses A, B, I, J, K, and external.
26	ADDR[12:15]	ADDR[12:15]
27		Reserved
28		Reserved
29		Reserved
30	Test Slave Mode Enable	Test Slave Mode Disabled
31	Test Transparent Mode Enable	Test Transparen Disabled

2.2.10.1 Chip Select Dip Switch (DS1)

The MPC505 MCU uses several chip selects on- peripheral devices). You can redefine these cl expansion connectors. To avoid conflicts betw appropriate chip select by setting the appropriate

Table 2-6. Chip Sele

Pin	Chip Select	D
1	CSBOOT	Flash chip select (U
2	FOE	Flash output enable
3	CS1	Burst RAM Bank1 (
4	CS2	Burst RAM Bank2 (
5	CS3	Burst RAM Bank3 (
6	CS4	Burst RAM Bank4 (
7	CS5	SCSI DUART (U4)
8	—	UNUSED

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

Freescale Semiconductor, Inc.

2.3.10.2 Reset Data Dip Switches (DS2 –

Dip switches DS2 – DS5 are connected through
D0). At RESET the MCU reads the data bus a
switches ("ON" = 0 LOGIC).

There are two reset configuration modes: data b
internal default mode. In either mode the configu
word onto the internal data bus. Table 2-7 descri
Mode column shows the default reset conf
configuration word is X9E5EF4A3. For inform
refer to the PowerPC MPC505 RISC Microcontr

Table 2-7. Data Bus Re

Data Bus Bit	Configuration Function Effected	Effect o Mode Selec During Re
0	Address Bus	Minimum Bus M ADDR[0:11] = C
1	Vector Table Location (IP Bit)	Vector Table 0xFFF0 0000
2	Burst Type/Indication	Type 2/LAST
3	Interface Type for CSBOOT	ITYPE = 001 Asynchronous (T Hi-Z = 2Clk)
4	CSBOOT Port Size	32-Bit
5	Reset Configuration Source For DATA[6:13]	Latch Configurat external pins.
[6:8]	TA Delay For CSBOOT	TA Delay Encod 000 001 010 011 100 101 110 111

Table 2-7. Data Bus Reset Co

Data Bus Bit	Configuration Function Effected	Effect o Mode Selec During Re
[9:10]	IMEMBASE[0:1]	IMEMBASE 00 01 10 11
[11:12]	LMEMBASE[0:1]	LMEMBASE 00 01 10 11
13	Reset configuration source for DATA[14:21]	Latch configurati external pins
14	CT[0:3], AT[0:1], TS	CT[0:3], AT[0:1],
15	WR, BDIP	WR, BDIP
16	PLLL/DSDO, VF[0:2], VFLS[0:1], WP[1:5]	DSDO, Pipe Trac Watchpoints
17	BURST, TEA, AACK, TA, BE[0:3]	Handshake Pins
18	CR, BI, BR, BB, BG, ARETRY	Bus Arbitration P
19	Release reset when PLL locked	Release reset wh locked and after (when not in PLL mode)
20		Reserved
21	Reset Configuration Source For DATA[22:31]	Latch Configurat external pins.
22		Reserved
23	IEN	I-bus Memory mo are enabled.

Freescale Semiconductor, Inc.

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

2.3.3 Power Supply – EVB Interconnection

The EVB requires +5 Vdc @ 2 amp power supp
pins 2 and 3 are ground (shown in Figure 2-2). U
with the board). EVB power supply interconnect

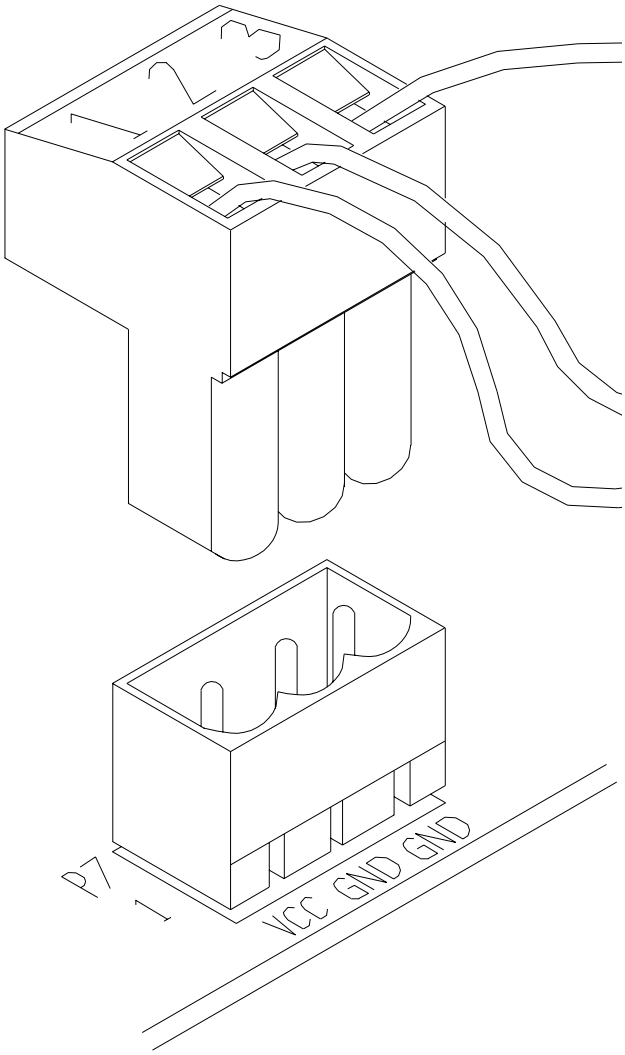


Figure 2-2. Power Su

2.2.10.3 DTE/DCE Settings

DS6 switch 1 lets you define which connecto
switches 2 - 4 lets you define I/O connectors P2
DS6 switch settings.

Table 2-8. DS6 Communic

Pin #	Signal Name	Connector	
1	OEDSDIDSCK	P4/P5	Swi Swi I/O
2	ADCE_DTE~	P2	ON OFI
3	BDCE_DTE~	P3	ON OFI
4	CDCE_DTE~	P4	ON OFI
5	—		
6	—		
7	—		
8	—		

Freescale Semiconductor, Inc.

For More Information On This Product,
Go to: www.freescale.com

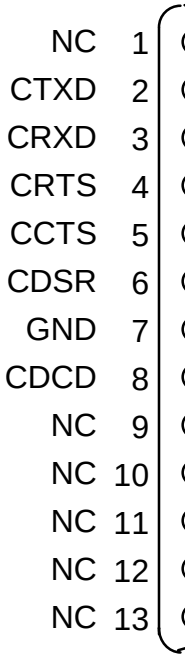
Freescale Semiconductor, Inc.

2.3 INSTALLATION INSTRUCTION

The EVB is designed for table top operation. A
(with an RS-232C port) are required for EVB op

2.3.1 Host Computer – EVB Interconnectio

Interconnection of a host computer to the EVB
cable assembly. One end of the cable assembly
below). The other end of the cable assembly is c
assignments and signal descriptions of the EVB

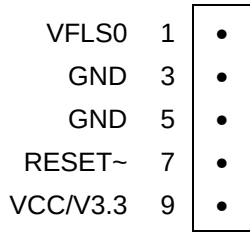


HOST C

2.3.2 Background Mode Connector (P5)

Use connector P5 (pinouts shown below) to c
debug mode (BDM). You may use the serial dev
Connect one end of the SDI to your host com
information about the SDI refer to the M68SDIU

P



For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

Freescale Semiconductor, Inc.

2.3.6 Logic Analyzer Connectors

Use connectors POD1 through POD7 to connec
Below are the pin assignments for the logic analy

POD1

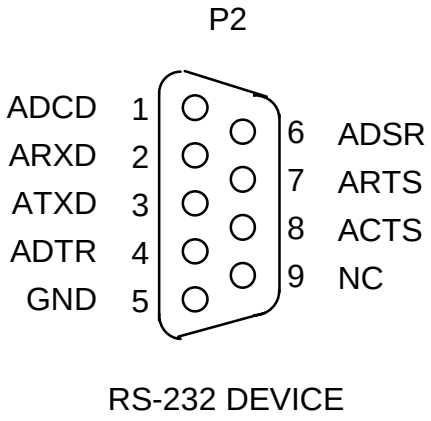
NC	1	•	•	2	NC
TS~	3	•	•	4	FOE~
CS1~	5	•	•	6	CS2~
CS3~	7	•	•	8	CS4~
CS5~	9	•	•	10	BSWE0~
BSWE1~	11	•	•	12	BSWE2~
BSWE3~	13	•	•	14	A10
A11	15	•	•	16	A12
A13	17	•	•	18	A14
A15	19	•	•	20	GND

POD3

NC	1	•	•	2	NC
NC	3	•	•	4	D16
D17	5	•	•	6	D18
D19	7	•	•	8	D20
D21	9	•	•	10	D22
D23	11	•	•	12	D24
D25	13	•	•	14	D26
D27	15	•	•	16	D28
D29	17	•	•	18	D30
D31	19	•	•	20	GND

2.3.4 RS-232C – EVB Interconnection

Interconnection of an RS-232C compatible de
supplied 9-pin cable assembly. One end of the ca
or P3 (shown below). The other end of the cable
232C compatible device. For connector pin assig
232C ports P2 and P3, refer to Appendix B.



Freescale Semiconductor, Inc.

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

2.3.5 EVB Expansion Connectors

There are two expansion connectors (P6 and P
expansion connectors are in Figures 2-3 and 2-4.

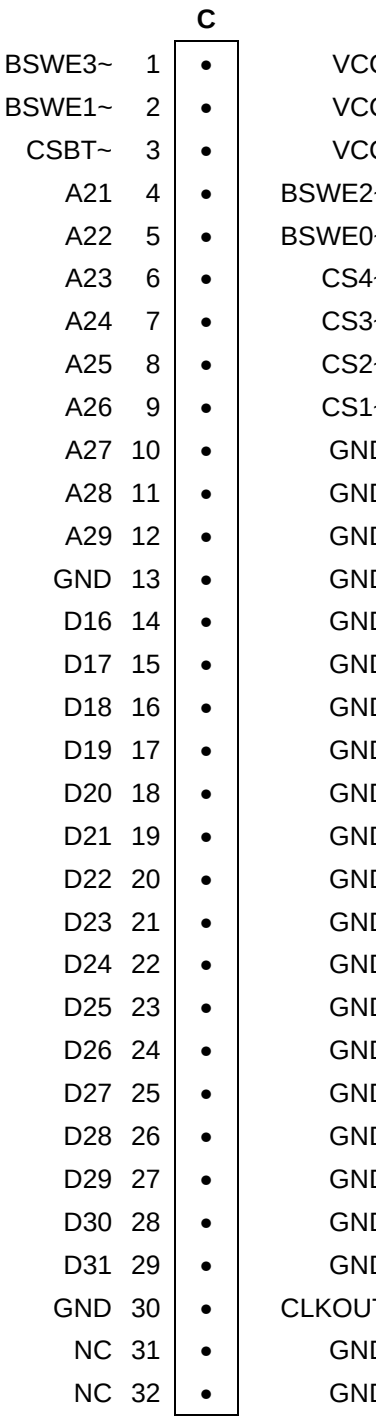


Figure 2-3. Expansion Con

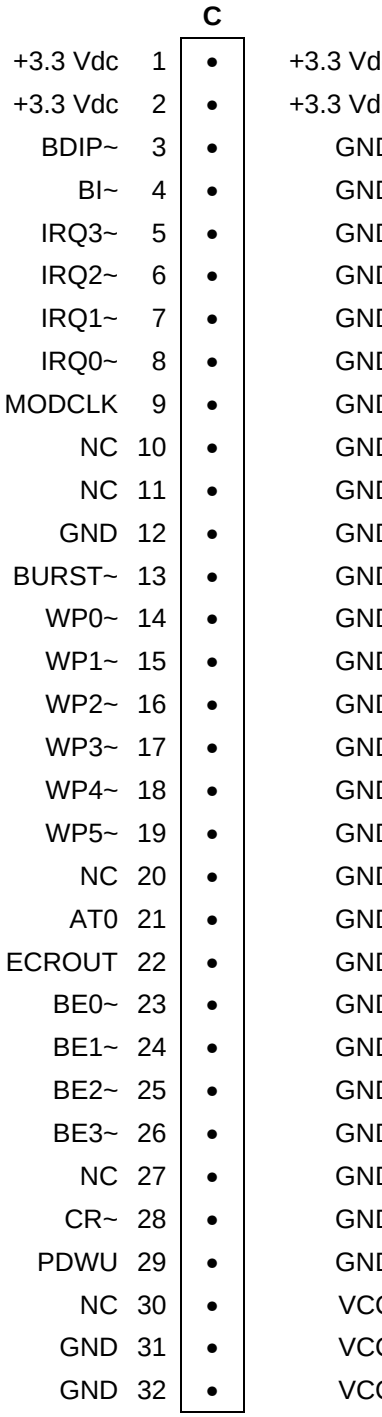

C
+3.3 Vdc 1 • +3.3 Vd
+3.3 Vdc 2 • +3.3 Vd
BDIP~ 3 • GND
BI~ 4 • GND
IRQ3~ 5 • GND
IRQ2~ 6 • GND
IRQ1~ 7 • GND
IRQ0~ 8 • GND
MODCLK 9 • GND
NC 10 • GND
NC 11 • GND
GND 12 • GND
BURST~ 13 • GND
WP0~ 14 • GND
WP1~ 15 • GND
WP2~ 16 • GND
WP3~ 17 • GND
WP4~ 18 • GND
WP5~ 19 • GND
NC 20 • GND
AT0 21 • GND
ECROUT 22 • GND
BE0~ 23 • GND
BE1~ 24 • GND
BE2~ 25 • GND
BE3~ 26 • GND
NC 27 • GND
CR~ 28 • GND
PDWU 29 • GND
NC 30 • VC
GND 31 • VC
GND 32 • VC

Figure 2-4. Expansion Con

Freescale Semiconductor, Inc.

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

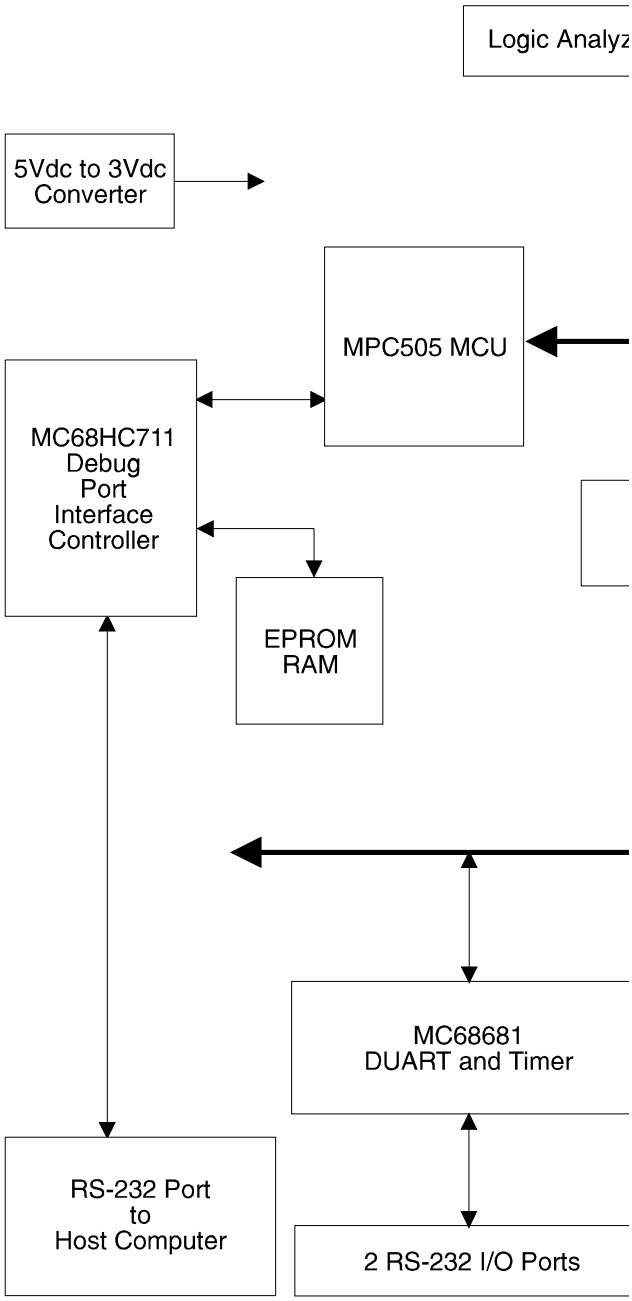


Figure 3-1. EVE

POD5

NC	1	•	•	2	NC
NC	3	•	•	4	DSCK
DSDI	5	•	•	6	DSDO
VF0	7	•	•	8	VF1
VF2	9	•	•	10	VFLS0
VFLS1	11	•	•	12	WP0~
WP1~	13	•	•	14	WP2~
WP3~	15	•	•	16	WP4~
WP5~	17	•	•	18	NC
NC	19	•	•	20	GND

POD7

NC	1	•	•	2	NC
CLKOUT	3	•	•	4	BURST~
TEA~	5	•	•	6	AACK~
TA~	7	•	•	8	BE0~
BE1~	9	•	•	10	BE2~
BE3~	11	•	•	12	BDIP~
R_W~	13	•	•	14	TS~
AT0	15	•	•	16	AT1~
BI~	17	•	•	18	ARETRY~
CSBT~	19	•	•	20	GND

2.3.7 SCSI

The EVB printed circuit board includes an optic
port are user supplied. SCSI port parts list is prov

Table 2-9. SCSI

Reference Designation	
P1	SCSI Conn
U1, U2	I.C., DS210 Semicondu
U3	I.C., 53C90

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

Freescale Semiconductor, Inc.

CHAP

FUNCTIONAL

3.1 INTRODUCTION

This chapter is a functional description of the EV

3.2 EVB DESCRIPTION

The EVB may be configured in either of two w
mounted on the target system. Figure 3-1 is the E

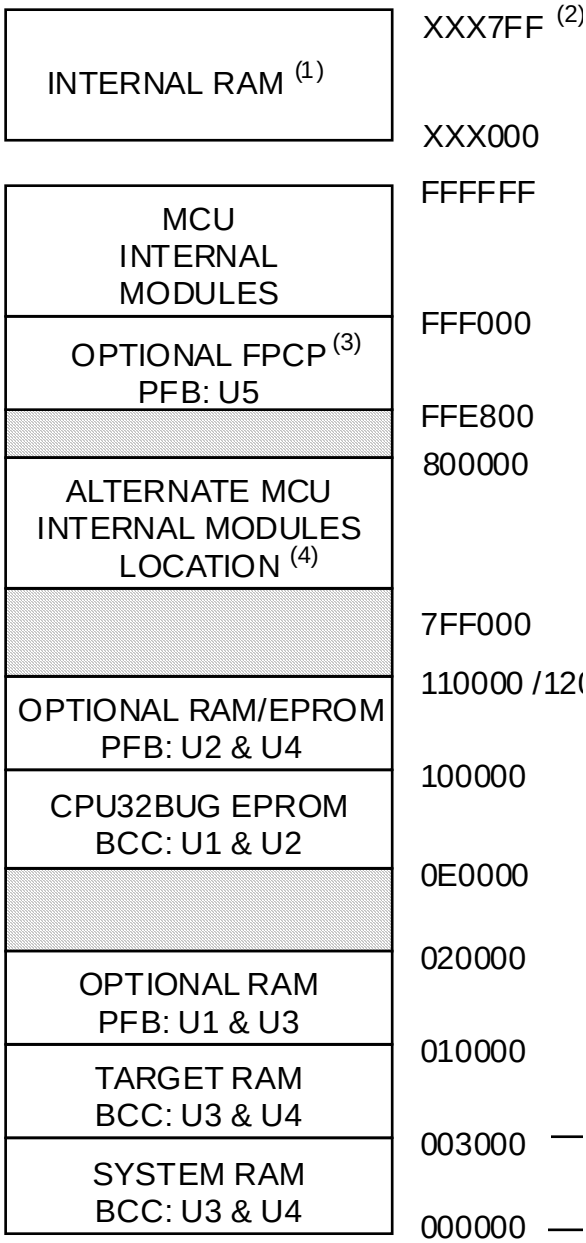
When the BCC is mounted on the PFB, you ma
code. To do this connect a terminal or host com
debug monitor program. Logic analyzer connecti
the PFB.

Mount the BCC on the target system to verify h
target system, MC68332 MCU device emulat
connecting a PC to BCC connector P4 and ru
connection may be made to connectors P1 and P

Freescale Semiconductor, Inc.

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.



1. Consult the MCU device user's manual.
2. XXbase address is user programmable. Interna internal RAM, can be configured on power-up/ initilization table (INITTBL) covered in Ap M68MPCBUG Debug Monitor User's Manual, M6
3. Floating point coprocessor - MC68881/MC68882.
4. See Appendix C of the M68MPCBUG Debug Mo M68MPCBUG /AD1.
5. Depends on the memory device type used.

Figure 3-2. EV

3.3 MCU SUMMARY

The resident MC68332 Microcontroller Unit designing, debugging, and evaluating MC68332 evaluation of prototype hardware/software produ

The MCU device is a 32-bit integrated micr manipulation capabilities with powerful peripher

- 32-bit central processor unit (CPU32)
- Time processor unit (TPU)
- Queued serial module (QSM)
- Random access memory (RAM)
- External bus interface
- Chip selects
- System clock
- Test module

3.3.1 32-Bit Central Processor Unit

The CPU32 is the central processor for the MC object code compatible with the MC68000 and unchanged. The CPU32 features are:

- 32-Bit internal data path and arithmet
- 32-Bit internal address bus - 24-bit ex
- Powerful instruction set
- Eight 32-bit general purpose data regi
- Seven 32-bit general purpose address
- Separate user and supervisor stack po
- Separate program and data address sp
- Flexible addressing modes
- Full interrupt processing

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

Freescale Semiconductor, Inc.

3.3.2 Time Processor Unit

The Time Processor Unit (TPU) optimizes perfo
dedicated execution unit, tri-level prioritized sch
microcode ROM which drastically reduces the
sixteen independent, orthogonal channels; eac
perform any time function. Each channel also co
and input capture functions.

Each channel can be synchronized to either of tw
One counter, based on the system clock, provide
The second counter, based on an external refe
clock divided by 8. Channels may also be li
operations on one channel to the occurrence of
inter-task control.

3.3.3 Queued Serial Module

The QSM contains two serial ports. The queued
easy peripheral expansion or inter-processor c
three-line bus: data-in, data-out, and a serial cl
provide address-ability for as many as 16 peripl
queue in a small RAM. This lets the QSPI hand
each, or to transmit a stream of data as long as
wrap-around mode lets the user continuously sa
the QSPI RAM for efficient interfacing to seri
converters).

The serial communications interface (SCI) port
mark/space format. Advanced error detection cir
in duration. Word length is software selectable l
baud rate generator provides baud rates from 6
clock. The SCI features full- or half-duplex op
enable bits and double buffering of data. Option
even or odd parity check capability. Wake-up fu
a true idle line is detected or a new address byte

3.3.4 Random Access Memory

2k bytes of static RAM are contained within the
storage of variable and temporary data. RAM d
32-bits (longword). The RAM can be mapped to

3.3.5 External Bus Interface

The external bus consists of 24 address lines and
sizing between 8- and 16-bit data accesses. A
bus cycle interruption. External bus arbitration
interface.

3.3.6 Chip Selects

Twelve independently programmable chip selec
peripheral access. Block size is programmable
can be selected for either 8- or 16-bit transfers. A
insertion during the access. All bus interface sig
logic.

3.3.7 System Clock

An on-chip phase locked loop circuit generates
16.78 MHz from a 32.768 kHz watch crystal.
providing either high performance or low po
system clock is a fully-static CMOS design, so i
via a low power stop instruction, while still reta
RAM.

3.3.8 Test Module

The test module consolidates the microcontrol
production testing, user self-test, and system di
provide signature analysis checks on internal log
pin to enter test mode. This test provides a pass
vectors.

3.4 USER MEMORY

On board the BCC is 32k x 16 bits of RAM a
debug monitor storage area and user accessib
Monitor is stored in the BCC EPROMs. For deb
Debug Monitor User's Manual, M68MPCBUG /

The PFB has sockets for 32k x 16 or 64k x 16
and/or EPROM, supplied by the user, is user-acc

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

Freescale Semiconductor, Inc.

Table 4-1. SCSI Conn

Pin	Mnemonic	
1	GND	GROUND
2	SDB0	SCSI DATA BUS (bi
3	GND	GROUND
4	SDB1	SCSI DATA BUS (bi
5	GND	GROUND
6	SDB2	SCSI DATA BUS (bi
7	GND	GROUND
8	SDB3	SCSI DATA BUS (bi
9	GND	GROUND
10	SDB4	SCSI DATA BUS (bi
11	GND	GROUND
12	SDB5	SCSI DATA BUS (bi
13	NC	Not Connected
14	SDB6	SCSI DATA BUS (bi
15	GND	GROUND
16	SDB7	SCSI DATA BUS (bi
17	GND	GROUND
18	SDBP	SCSI DATA BUS PA
19 – 25	GND	GROUND
26	VCC	+5 VDC POWER – I logic circuits.

3.5 I/O CONNECTORS

There are two 64-pin expansion connectors on th the BCC communicates with the PFB or target sy through P3 and serial communication through P4 interface connectors pin assignments.

3.5.1 64-Pin Expansion Connectors

The expansion connectors interconnect the BCC MC68332 MCU device, serial communication, a the expansion connectors.

3.5.2 Serial Communication Connectors

A terminal or host computer with terminal emula be connected to the BCC or to the PFB. Termi communication connectors, BCC P4 or to PFB P

3.5.3 Background Mode Interface Connect

The background debug mode is implemented in can be viewed or altered, memory can be read Background mode is initiated by one of seve internal peripherally generated breakpoints, so Instruction execution is suspended for the dur communications between the BCC and the devel

3.6 PFB DESCRIPTION

The PFB is the physical location for installing th memory. I/O connectors are available for commu

3.6.1 Floating-Point Coprocessor Socket (U

Socket U5 on the PFB accommodates an optiona or an MC68882 coprocessor can be used in sock part of the EVB, so must be provided by the interface, see the application note MC68881 Fl M68000 System, AN947.

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

Freescale Semiconductor, Inc.

The coprocessor interface is a transparent, log registers and instructions. To the external env model appear to be on the same chip.

A coprocessor interface is an execution model t CPU and coprocessor. For optimum performan instructions execute concurrently with CPU execution is further extended by the coproc instructions simultaneously.

3.6.2 Logic Analyzer Connectors

To debug hardware and software developed fc analyzer to the desired pins of PFB connectors P

CHAP

SUPPORT IN

4.1 INTRODUCTION

The tables in this chapter describe EVB connecto

4.2 CONNECTOR SIGNAL DESCRI

The following are all the connectors on the bo description.

Connector P7 connects external power to the E P4. POD1 through POD7 let you connect a logi ports for evaluating RS-232C devices.

NO

The signal descriptions in the reference only. For a complete consult the appropriate MCU user summary. For a complete descrip the appropriate NCR 53C90B U complete description of the P2,P MOTOROLA M68681 User Man

Tables 4-1 through 4-19 list pin assignments for

Table 4-1	SCSI connector P1 (not populated)
Table 4-2	RS-232C I/O port P2
Table 4-3	RS-232C I/O port P3
Table 4-4	Host computer connector P4
Table 4-5	Debug mode connector P5
Table 4-6	Expansion connector P6
Table 4-7	Input power connector P7
Table 4-8	Expansion connector P8

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

Freescale Semiconductor, Inc.

Table 4-4. Host Computer C

Pin	Mnemonic	
1	NC	Not Connected
2	CTXD	TRANSMIT – RS-23
3	CRXD	RECEIVE DATA – R
4	CRTS	REQUEST TO SENI transfer data.
5	CCTS*	CLEAR TO SEND – data status.
6	ADSR*	DATA SET READY - line/in-service/active
7	GND	GROUND
8	CDCD*	DATA CARRIER DE acceptable received
9 - 19	NC	Not Connected
20	ADTR*	DATA TERMINAL R service/active status
21 - 25	NC	Not Connected

Table 4-1. SCSI Connector

Pin	Mnemonic	
27 – 31	GND	GROUND
32	ATNI*	ATTENTION – Activ the MPC505 has a m
33 – 35	GND	GROUND
36	BSY	BUSY – Active low I/
37	GND	GROUND
38	ACK	ACKNOWLEDGE – target that the MPC5
39	GND	GROUND
40	RST	RESET – Active-low devices using the bu
41	GND	GROUND
42	MSG	MESSAGE – Active- sending a message.
43	GND	GROUND
44	SEL	SELECT – Active-lo target.
45	GND	GROUND
46	C/D	CONTROL/DATA – control of data is on
47	GND	GROUND
48	REQ	REQUEST – Active- that the target has tr
49	GND	GROUND
50	I/O	INPUT/OUTPUT – A controls data directio

Freescale Semiconductor, Inc.

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

Table 4-2. RS-232C I/O Co

Pin	Mnemonic	
1	ADCD*	DATA CARRIER DE acceptable received
2	ARXD	RECEIVE DATA – R
3	ATXD	TRANSMIT – RS-23
4	ADTR*	DATA TERMINAL R service/active status
5	GND	GROUND
6	ADSR*	DATA SET READY - line/in-service/active
7	ARTS	REQUEST TO SENI transfer data.
8	ACTS*	CLEAR TO SEND – data status.
9	NC	Not Connected

Table 4-3. RS-232C I/O Co

Pin	Mnemonic	
1	BDCD*	DATA CARRIER DE acceptable received
2	BRXD	RECEIVE DATA – R
3	BTXD	TRANSMIT – RS-23
4	BDTR*	DATA TERMINAL R service/active status
5	GND	GROUND
6	BDSR*	DATA SET READY - line/in-service/active
7	BRTS	REQUEST TO SENI transfer data.
8	BCTS*	CLEAR TO SEND – data status.
9	NC	Not Connected

Freescale Semiconductor, Inc.

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

Table 4-8. P8 Expansion Connec

Pin	Mnemonic	
A-21	NC	Not Connected
A-22	ARETRY*	ADDRESS PHASE F the master needs to
A-23	BG*	BUS GRANT – Activ device has assumed
A-24	BR*	BUS REQUEST – A device requests bus
A-25	BB*	BUS BUSY – Active- master that indicates
A-26	RESET*	RESET – Active-low
A-27	SRESET*	SYSTEM RESET – A the EVB.
A-28, A-29	VFLS1, VFLS0	VISIBILITY FLUSH - many instructions ar clock cycle. Also indi
A-30	DSDI	DEVELOPMENT SE mode.
A-31	DSCK	DEVELOPMENT SE debug mode.
A-32	DSDO	DEVELOPMENT SE debug mode.
B-1, B-2	V3.3	+3.3 VDC POWER - converter for use by
B-3 B-29	GND	GROUND
B-30 B-32	VCC	+5 VDC POWER – I logic circuits.
C-1, C-2	V3.3	+3.3 VDC POWER - converter for use by
C-3	BDIP*	BURST DATA IN PR indicates the data be master.

Table 4-5. Debug Mode Co

Pin	Mnemonic	
1	VFLS0	VISIBILITY FLUSH background debug
2	SRESET*	SYSTEM RESET – asserted by the MC
3	GND	GROUND
4	DSCK	DEVELOPMENT SI debug mode.
5	GND	GROUND
6	VFLS1	VISIBILITY FLUSH background debug
7	RESET*	RESET – Active-lo
8	DSDI	DEVELOPMENT SI mode.
9	VCC	+5 VDC POWER – logic circuits.
10	DSDO	DEVELOPMENT SI debug mode.

Freescale Semiconductor, Inc.

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

Table 4-6. P6 Expansion C

Pin	Mnemonic	
A-1	FOE*	FLASH OUTPUT E the EVB on-board fl
A-2	CS5*	CHIP SELECT 5 Ou at programmed add
A-3 A-13	A10 A20	ADDRESS BUS (bi address bus.
A-14	GND	GROUND
A-15 A-30	D0 D15	DATA BUS (bits 0
A-31	GND	GROUND
A-32	NC	Not Connected
B-1 B-3	VCC	+5 VDC POWER –I logic circuits.
B-4	BSWE2*	Address signal A8 -
B-5	BSWE0*	Address signal A6 -
B-6 B-9	CS4* CS1*	CHIP SELECT (4 – devices at programı
B-10 B-29	GND	GROUND
B-30	CLKOUT	SYSTEM CLOCK C internal system cloc
B-31, B-32	GND	GROUND
C-1	BSWE3*	Address signal A9 -
C-2	BSWE1*	Address signal A7 -
C-3	CSBT*	BOOT CHIP SELEC or memory devices
C-4 C-12	A21 A29	ADDRESS BUS (bi bus.
C-13	GND	GROUND
C-14 C-29	D16 D31	DATA BUS (bits 16
C-30	GND	GROUND
C-31, C-32	NC	Not Connected

Table 4-7. Input Power Co

Pin	Mnemonic	
1	VCC	+5 VDC POWER – I logic circuits. The "V
2	GND	GROUND The "GND
3	GND	GROUND The "GND

Table 4-8. P8 Expansion C

Pin	Mnemonic	
A-1, A-2	V3.3	+3.3 VDC POWER – converter for use by
A-3	AACK*	ADDRESS ACKNOW the slave has receive
A-4	TS*	TRANSFER START start of a bus cycle.
A-5	VDDSYN	VDDSYN – Clock sy
A-6 A-8	IRQ6* – IRQ4*	INTERRUPT REQU requests MCU synch
A-9 A-12	CT0 CT3	CYCLE TYPE SIGN the bus master is init
A-13	GND	GROUND
A-14 A-16	VF0 VF2	VISIBILITY FETCH - fetched instruction o instruction queue.
A-17	R_W*	READ/WRITE – Acti data transfer on the
A-18	TA*	TRANSFER ACKNO indicates the slave h data during a read cy
A-19	TEA*	TRANSFER ERROR indicates bus error c
A-20	AT1	ADDRESS TYPES b space as: user data, instruction.

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

Freescale Semiconductor, Inc.

Table 4-14. Logic Analyzer Co

Pin	Mnemonic	
1 – 3	NC	Not Connected
4	CLKOUT	SYSTEM CLOCK O internal system clock
5	RESET*	RESET – Active-low
6	SRESET*	SYSTEM RESET – A the EVB.
7 – 10	CT0 – CT3	CYCLE TYPE SIGN the bus master is init
11	CR*	CANCEL RESERVA to clear the external
12	BR*	BUS REQUEST – A device requests bus
13	BB*	BUS BUSY – Active- master that indicates
14	BG*	BUS GRANT – Activ device has assumed
15, 16	IRQ0*, IRQ1*	INTERRUPT REQU requests MCU synch
17	ECROUT	ENGINEERING CLO peripheral chips.
18	MODCLK	CLOCK MODE SEL source of the interna
19	PDWU	POWER DOWN WA to external power-on
20	GND	GROUND

Table 4-8. P8 Expansion Connec

Pin	Mnemonic	
C-4	BI*	BURST INHIBIT – A not support burst mo
C-5, C-6	IRQ3* IRQ2*	INTERRUPT REQU requests MCU synch
C-7, C-8	IRQ1*, IRQ0*	INTERRUPT REQU requests MCU synch
C-9	MODCK	CLOCK MODE SEL source of the interna
C-10, C-11	NC	Not Connected
C-12	GND	GROUND
C-13	BURST*	BURST – Active low
C-14 C-17	WP0* – WP3*	WATCHPOINT (0 - 3 watchpoint.
C-18, C-19	WP4*, WP5*	WATCHPOINT (4, 5 watchpoint.
C-20	NC	Not Connected
C-21	AT0	ADDRESS TYPES b space as: user data, instruction.
C-22	ECROUT	ENGINEERING CLO peripheral chips.
C-23 C-26	BE0* BE3*	BYTE ENABLE (03) controls one byte lan
C-27	NC	Not Connected
C-28	CR*	CANCEL RESERVA to clear the external
C-29	PDWU	POWER DOWN WA to external power-on
C-30	NC	Not Connected
C-31, C-32	GND	GROUND

Freescale Semiconductor, Inc.

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

Table 4-9. Logic Analyzer Cor

Pin	Mnemonic	
1, 2	NC	Not Connected
3	TS*	TRANSFER START start of a bus cycle.
4	FOE*	FLASH OUTPUT EN the EVB on-board fla
5 – 9	CS1* – CS5*	CHIP SELECT (1 – 5 devices at programm
10 – 13	BSWE0* – BSWE3*	Address signal A6 - A bus.
14 – 19	A10 – A15	ADDRESS BUS (bits bus.
20	GND	GROUND

Table 4-10. Logic Analyzer Cor

Pin	Mnemonic	
1 – 3	NC	Not Connected
4 – 17	A16 – A29	ADDRESS BUS (bits bus.
18 – 20	GND	GROUND

Table 4-11. Logic Analyzer Cor

Pin	Mnemonic	
1 – 3	NC	Not Connected
4 – 19	D16 – D31	DATA BUS (bits 16
20	GND	GROUND

Table 4-12. Logic Analyzer Cor

Pin	Mnemonic	
1 – 3	NC	Not Connected
4 – 19	D0 – D15	DATA BUS (bits 0 1
20	GND	GROUND

Table 4-13. Logic Analyzer Cor

Pin	Mnemonic	
1 – 3	NC	Not Connected
4	DSCK	DEVELOPMENT SE debug mode.
5	DSDI	DEVELOPMENT SE mode.
6	DSDO	DEVELOPMENT SE debug mode.
7 – 9	VF0 – VF2	VISIBILITY FETCH - fetched instruction o instruction queue.
10, 11	VFLS0, VFLS1	VISIBILITY FLUSH - many instructions ar clock cycle. Also indi
12 – 15	WP0* – WP3*	WATCHPOINT (0 - 3 watchpoint.
16, 17	WP4*, WP5*	WATCHPOINT (4, 5 watchpoint.
18, 19	NC	Not Connected
20	GND	GROUND

Freescale Semiconductor, Inc.

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

Table 4-15. Logic Analyzer Co

Pin	Mnemonic	
1, 2	NC	Not Connected
3	CLKOUT	SYSTEM CLOCK O internal system clock
4	BURST	BURST – Active low
5	TEA*	TRANSFER ERROR indicates bus error c
6	AACK*	ADDRESS ACKNOW the slave has receive
7	TA*	TRANSFER ACKNO indicates the slave h data during a read cy
8 – 11	BE0* – BE3*	BYTE ENABLE (0 3 controls one byte lan
12	BDIP*	BURST DATA IN PR indicates the data be master.
13	R_W*	READ/WRITE – Acti data transfer on the
14	TS*	TRANSFER START start of a bus cycle.
15, 16	AT0, AT1	ADDRESS TYPES (space as: user data, instruction.
17	BI*	BURST INHIBIT – A not support burst mo
18	ARETRY*	ADDRESS PHASE R the master needs to
19	CSBT*	BOOT CHIP SELEC or memory devices a
20	GND	GROUND

Freescale Semiconductor, Inc.

For More Information On This Product,
Go to: www.freescale.com